NCP1526

3 MHz, 400 mA, High-Efficiency, Step-Down Converter with Low Noise Voltage Regulator Optimized to Power Application Processor or RF Module

The NCP1526 is a monolithic integrated circuit combining a step−down PWM DC−DC converter and a low noise, low dropout voltage regulator. The device is dedicated to power RF sensitive module in portable applications from one Li−ion or three Alkaline / NiCd / NiMH batteries cells. The DC−DC converter offers fixed output voltage and delivers up to 400 mA. It uses synchronous rectification to increase efficiency and eliminates the external Schottky diode.

The device also has a built−in 3.0 MHz (nominal) oscillator which reduces component size by allowing the use of small inductor (down to 1 μH) and capacitors. Additional features include integrated soft−start, cycle−by−cycle current limiting, and thermal shutdown protection. The integrated very low noise, low dropout regulator is available with 150 mA current capability, current limitation and temperature limit protection.

The NCP1526 is available in a space saving, ultra low profile 3x3 mm, 10 pin UDFN package (thickness 0.55 mm max).

Features

- Step−Down Converter
  - Up to 94% Efficiency (85% at 1.2 V)
  - Output Current Capability 400 mA
  - 3.0 MHz Switching Frequency
  - Fixed Output Voltage (1.2 V available now, other voltages available upon request) (see page 13)
  - Synchronous Rectification for Higher Efficiency
- LDO Regulator
  - Fixed Output Voltage (2.8 V available now, other voltages available upon request) (see page 13)
  - Up to 150 mA Output Current Capability
  - Very Low Noise: 45 μV_{RMS}
- All Pins are Fully ESD Protected
- 2.7 V to 5.2 V Input Voltage Range
- Thermal Limit Protection
- 3.0 mm x 3.0 mm x 0.55 mm UDFN Package
- This is a Pb−Free Device

Typical Applications

- Cellular Phones, Smart Phones and PDAs
- Digital Still Cameras
- MP3 Players and Portable Audio Systems
- Wireless and DSL Modems
- Portable Equipment

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http://onsemi.com

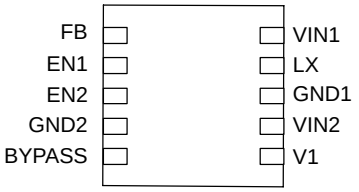
10 PIN DFN
MU SUFFIX
CASE 506AT

MARKING DIAGRAM

1526	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1526MUTXG	UDFN−10 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

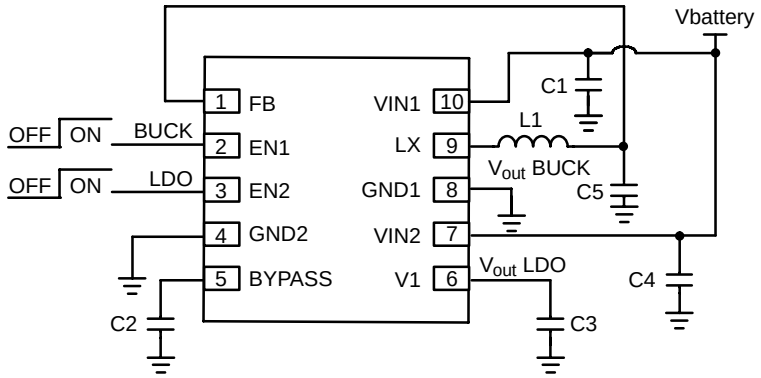


Figure 1. Typical Applications Circuit

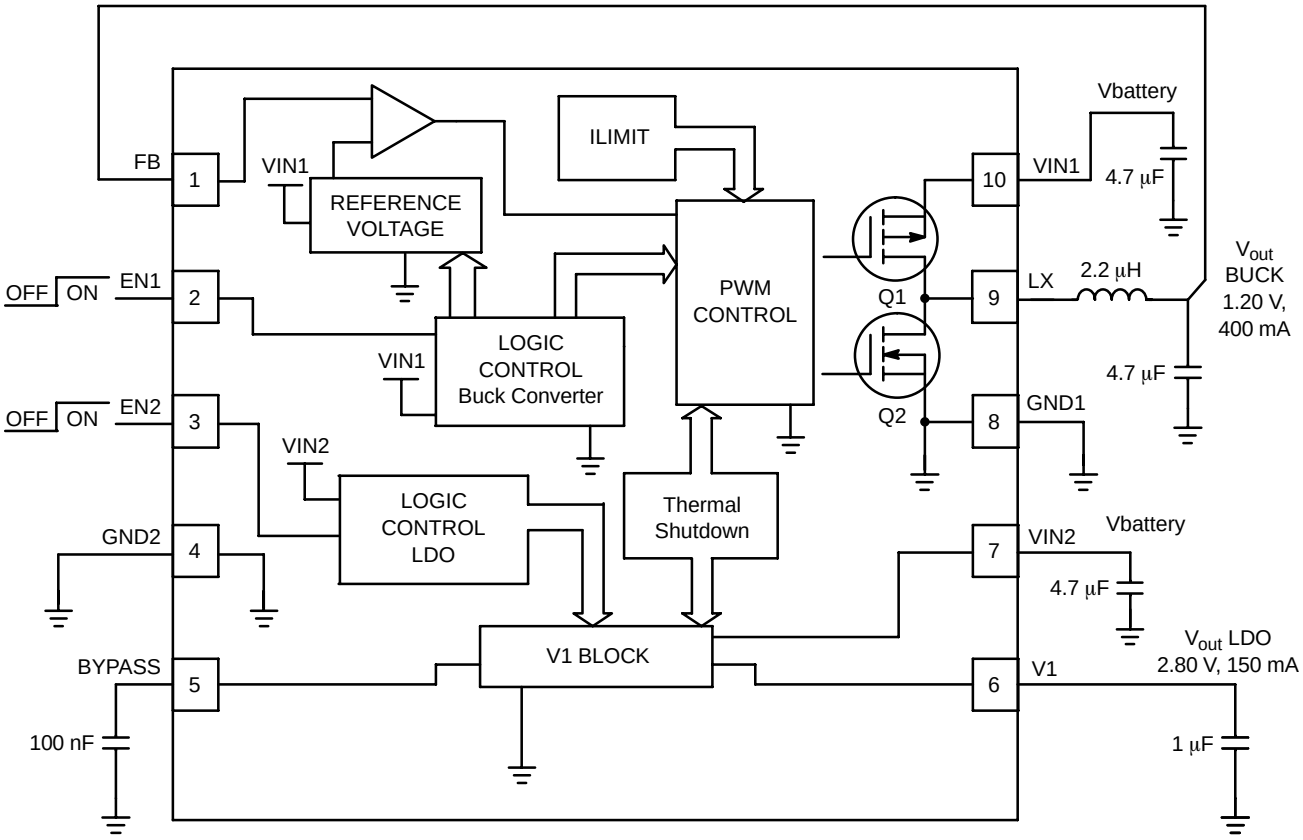


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION (Pin out provided for concept purpose only and might change in the final product.)

Pin No.	Symbol	Function	Description
1	FB	Analog Input	Feedback voltage from the output of the power supply. This is the input to the error amplifier.
2	EN1	Digital Input	Enable for DC−DC converter. This pin is active high. It is turned off by logic LOW on this pin. Do not float this pin.
3	EN2	Digital Input	EN2 enables the LDO.A HIGH level on this pin activates the voltage regulator. It is turned off by logic LOW on this pin. Do not float this pin.
4	GND2	Power Ground	Ground connection for the LDO section and must be connected to the system ground.
5	BYPASS		Bypass is the bandgap reference for the LDO. This pin requires a 100 nF bypass capacitor for low noise. This pin cannot be used for an external source.
6	V1	Output Power	This pin provides the output voltage supplied by the LDO. This pin requires 1.0 μF decoupling capacitor.
7	VIN2	Power Input	Input battery voltage to supply voltage regulator blocks. The pin requires a 4.7 μF decoupling capacitor.
8	GND1	Power Ground	This pin is the GROUND reference for the DC−DC converter and the output control. The pin must be connected to the system ground.
9	LX	Analog Output	Connection from Power MOSFETs to the inductor. An output discharge circuit sinks current from this pin.
10	VIN1	Power Input	Input battery voltage to supply the analog and digital blocks of the DC−DC converter. The pin must be decoupled to ground by a 4.7 μF ceramic capacitor.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage All Pins	V_{min}	−0.3	V
Maximum Voltage All Pins (Note 2)	V_{max}	7.0	V
Maximum Voltage EN1, EN2, FB, LX	V_{max}	VIN + 0.3	V
UDFN10 Package (Note 5) Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	240	°C/W
Operating Ambient Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C
Junction Operating Temperature	T_J	−40 to 125	°C
Latch−up Current Maximum Rating (T_A = 85°C) (Note 4) FB pin Other pins	Lu	±70 ±100	mA
ESD Withstand Voltage (Note 3) Human Body Model Machine Model	Vesd	 2.0 200	 kV V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) per JEDEC standard: JESD22−A114.
   Machine Model (MM) per JEDEC standard: JESD22−A115.
4. Latchup current maximum rating per JEDEC standard: JESD78.
5. The exposed flag shall be connected to ground.
6. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS, DC/DC Converter (Typical values are referenced to T_A = +25°C, Min and Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted, operating conditions V_{IN} = 3.6 V, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
VIN1 PIN						
Input Voltage Range	10	V_{in}	2.7	−	5.2	V
Quiescent Current, I_{out} = 0 mA, No Switching Quiescent Current, I_{out} = 0 mA, Oscillator Running	8	$I_{q\ ON}$	− −	250 2.5	350 −	μA mA
Quiescent Current, EN Low	8	$I_{q\ OFF}$	−	0.2	1.5	μA
Undervoltage Lockout (V_{IN} Increase)	10	V_{UVLO}	−	2.5	−	V
Undervoltage Lockout Hysteresis	10	V_{HUVLO}	−	100	−	mV
EN1, EN2 PIN						
Positive Going Input High Voltage Threshold, EN0 Signal	2, 3	V_{IH}	1.2	−	−	V
Negative Going Input High Voltage Threshold, EN0 Signal	2, 3	V_{IL}	−	−	0.4	V
DC−DC CONVERTER SECTION						
Peak Inductor Current	9	I_{LIM}	−	1000	−	mA
Feedback Voltage Threshold Overtemperature	1	V_{FB}	 1.164	 1.2	 1.236	V
Load Transient Response, Rise/Fall Time 1.0 μs 1.0 mA to 300 mA Load Step 1.0 mA to 400 mA Load Step	−	V_{OUT}	 − −	 30 35	 − −	mV
Line Transient Response, I_{out} = 100 mA, 3.0 V to 3.6 V Line Step	−	V_{OUT}	−	±5.0	−	mVpp
Output Voltage Load Regulation I_{out} = 1.0 mA to 300 mA I_{out} = 1.0 mA to 400 mA	−	V_{OUT}	 − −	 0.2 0.5	 − −	%
Output Voltage Line Regulation, I_{out} = 100 mA, V_{IN} = 2.7 V to 5.2 V	−	V_{OUT}	−	0.1	−	%
Output Voltage Ripple, I_{out} = 300 mA	−	V_{OUT}	−	5.0	−	mV
Oscillator Frequency	9	F_{OSC}	2.4	3.0	3.6	MHz
P−Ch On−Resistance	1	RLxH	−	400	−	mΩ
N−Ch On−Resistance	1	RLxL	−	400	−	mΩ
P−Ch Leakage Current	1	ILeakH	−	0.05	−	μA
N−Ch Leakage Current	1	ILeakL	−	0.01	−	μA
Soft−Start Time	−	Tstart	−	100	300	μs

ELECTRICAL CHARACTERISTICS for LDO (Typical values are referenced to T_A = +25°C, Min and Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted, operating conditions 3 V < V_{IN} < 5.2 V, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
VIN2 PIN						
Input Voltage Range	7	V_{in}	3	−	5.2	V
Quiescent Current On State VIN2 = 4.2 V, I_{out} = 0 mA	4	$I_{q\ ON}$	−	70	95	μA
Quiescent Current Off State	4	$I_{q\ OFF}$	−	0.2	−	μA
LDO SECTION						
Output Voltage, I_{out} = 0 mA to 150 mA	6	V1	2.716	2.80	2.884	V
Maximum Output Current	6	I_{out}	150	−	−	mA
Output Voltage Line Regulation, I_{out} = 10 mA	6	V1	−	10	−	mV
Load Regulation, I_{out} = 1.0 mA to 150 mA, V_{IN} = 3.6 V	6	V1	−	20	−	mV
Power Supply Ripple Rejection on V1, (0.2 Vp−p), C_{out} = 1.0 μF, V_{in} = 3.6 V 1.0 kHz I_{out1} = 100 μA 100 kHz, I_{out1} = 100 μA	6	PSRR	 − −	 67 45	 − −	dB
Dropout Voltage, I_{out} = 150 mA		VINA−V1	−	−	150	mV
Output Short Circuit Current	6	ISC	250	300	−	mA
Output Noise Voltage, 100 Hz to 100 kHz, I_{out} = 10 mA, C_{out}= 1.0 μF	6	V_N	−	45	−	μVrms
Turn ON Output Voltage, V_{in} = 3.6 V	6	Ton	−	80	150	μs
BYPASS PIN						
Output Voltage, Cby = 100 nF	5	V_{BY}	−	1.5	−	V

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TYPICAL CHARACTERISTICS FOR STEP DOWN CONVERTER			FIGURE
η	Efficiency	vs. Load Current	3, 4
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V_{OUT}	Output Voltage	vs. Temperature	6
F_{OSC}	Frequency Variation	vs. Input Voltage	7
V_{OUT}	Load Regulation	vs. Load Current	5
V_{OUT}	Load Transient Response		12
V_{OUT}	Line Regulation	vs. Ouptput Current	9
		vs. Temperature	10
V_{OUT}	Line Transient Response		14
	PWM Mode Operation		13
Tstart	Soft Start		11

TYPICAL CHARACTERISTICS

NCP1526 circuit on Figure 2, V_{in} = 3.6 V, T_A = 25°C, unless otherwise noted

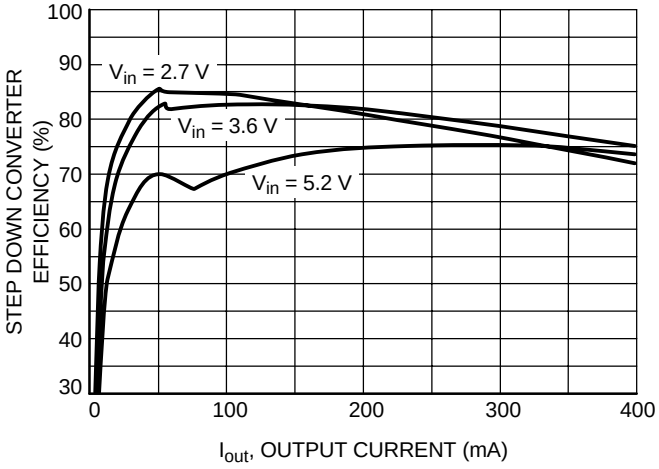

Figure 3. Step Down Converter Efficiency vs. Output Current

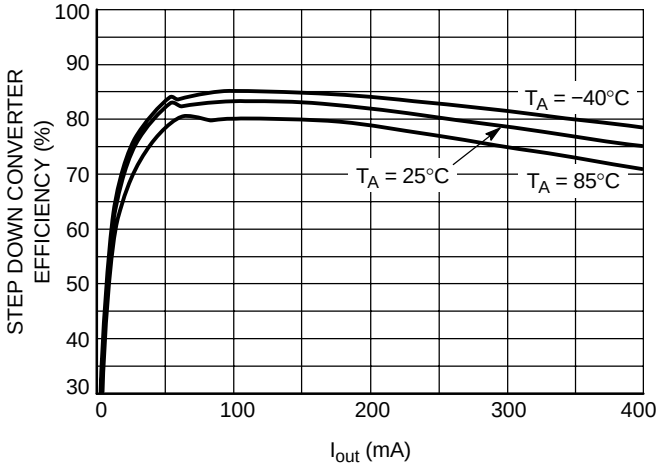

Figure 4. Step Down Converter Efficiency vs. Temperature V_{in} = 3.6 V

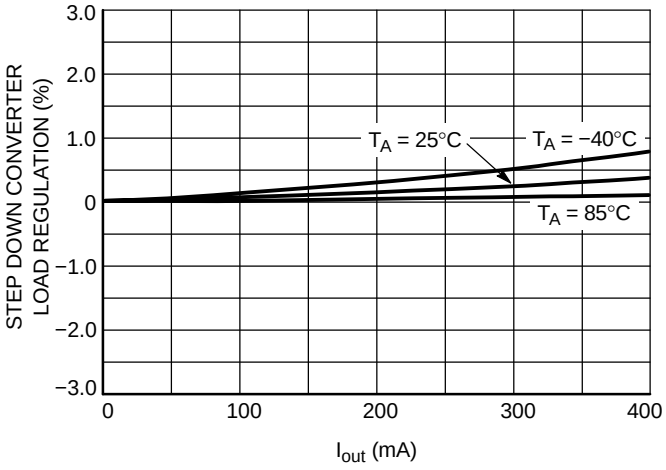

Figure 5. Step Down Converter Load Regulation vs. Temperature V_{in} = 3.6 V

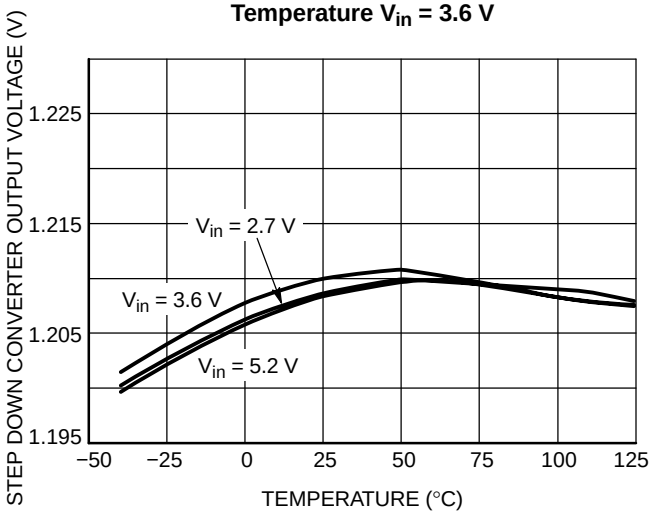

Figure 6. Step Down Converter Output Voltage vs. Temperature at I_{out} = 100 mA

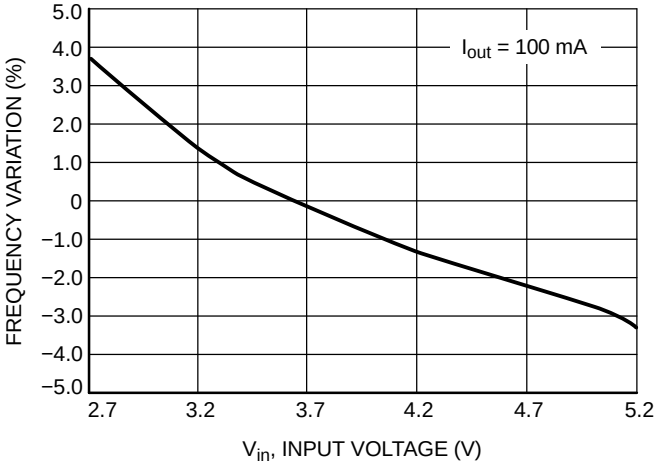

Figure 7. Step Down Converter Switching Frequency vs. Input Voltage

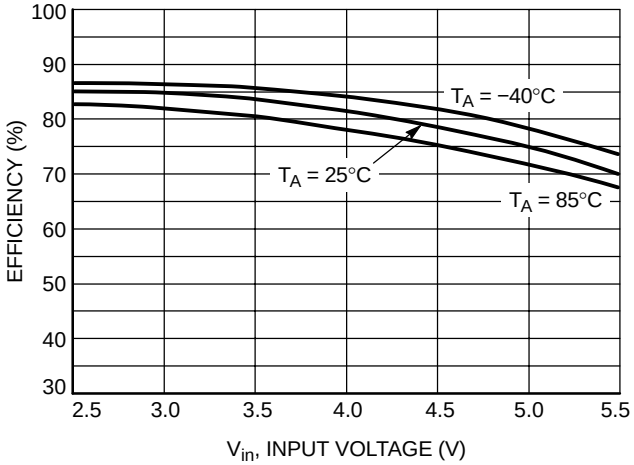

Figure 8. Step Down Converter Efficiency vs. Input Voltage at I_{out} = 100 mA

TYPICAL CHARACTERISTICS

NCP1526 circuit on Figure 2, V_{in} = 3.6 V, T_A = 25°C, unless otherwise noted

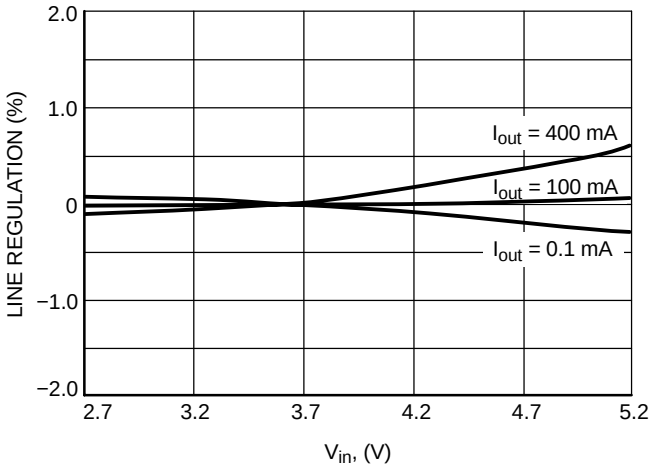

Figure 9. Step Down Converter Line Regulation vs. Output Current

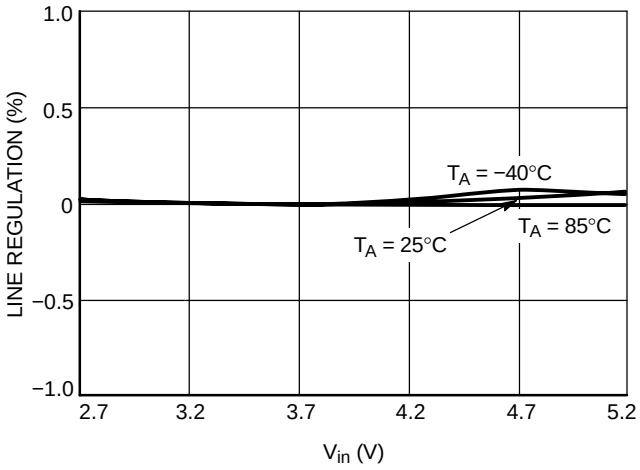

Figure 10. Step Down Converter Line Regulation vs. Temperature at I_{out} = 100 mA

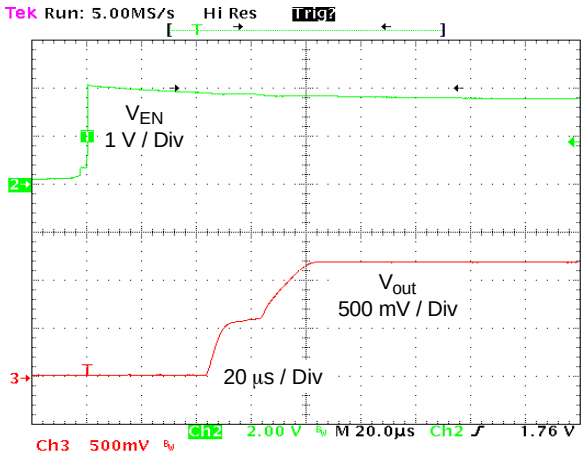

Figure 11. Step Down Converter Soft Start Time

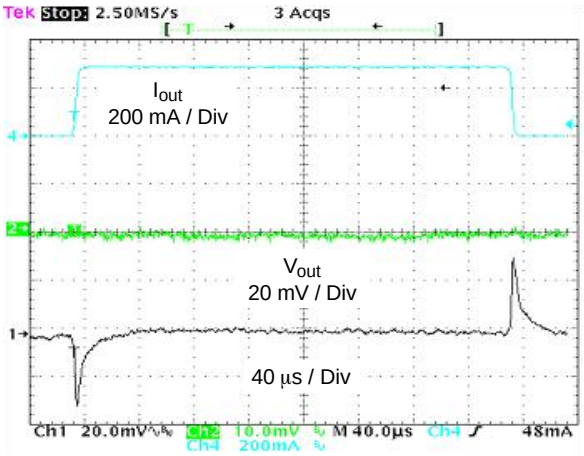

Figure 12. Step Down Converter Load Transient Response

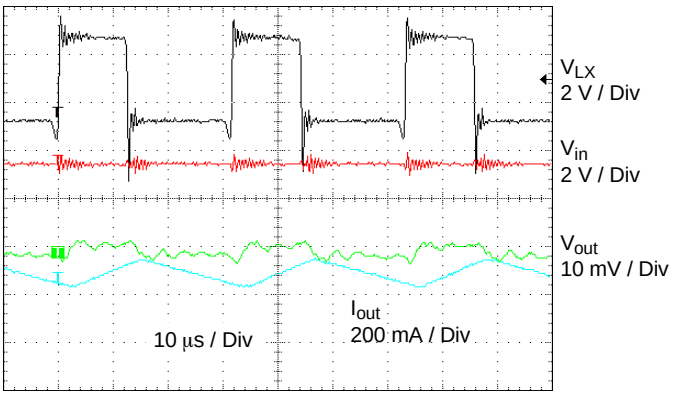

Figure 13. Step Down Converter PWM Mode of Operation

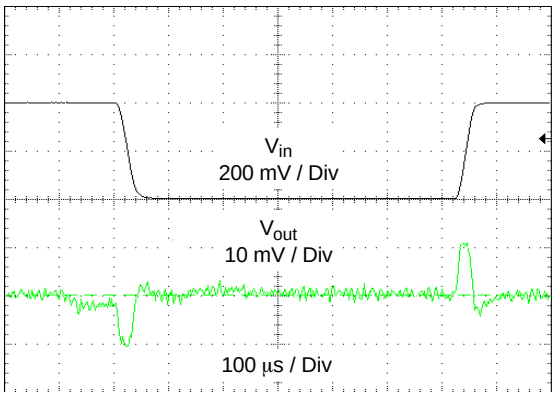

Figure 14. Step Down Converter Line Transient Response

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TYPICAL CHARACTERISTICS FOR LDO			FIGURE
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V1	Load Regulation	vs. Load Current	15, 16
	Load Transient Response		18
Iq_{ON}	Quiescent Current	vs. Input Voltage	19
T_{ON}	Turn On Time		17
V_N	LDO Noise	vs. Frequency	20, 21
PSRR	PSRR	vs. Frequency	23

TYPICAL CHARACTERISTICS

NCP1526 circuit on Figure 2, V_{in} = 3.6 V, T_A = 25°C, unless otherwise noted

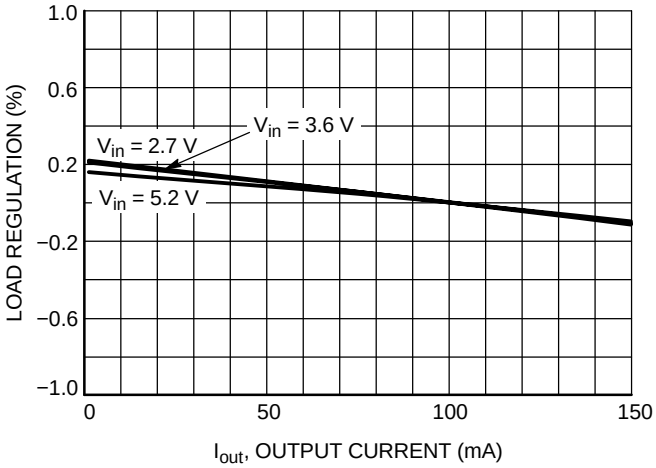


Figure 15. LDO Load Regulation

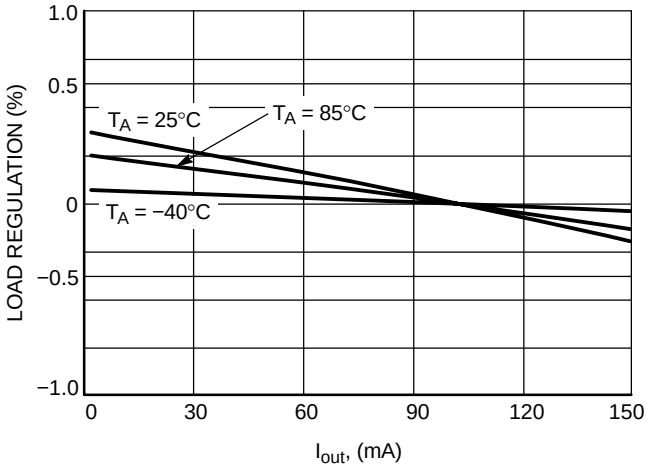


Figure 16. LDO Load Regulation vs. Temperature

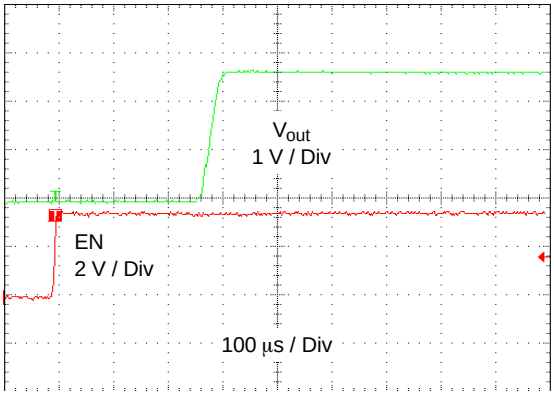


Figure 17. LDO Turn On Time from Enable

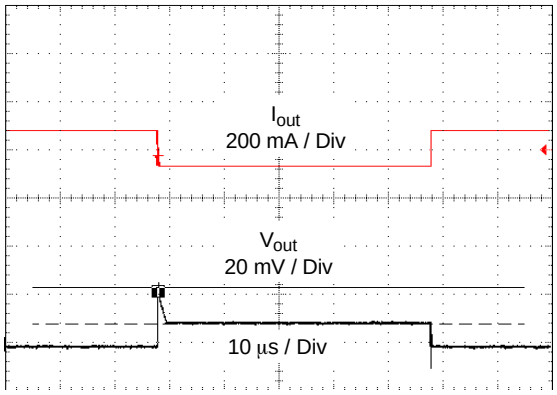


Figure 18. LDO Load Transient Response

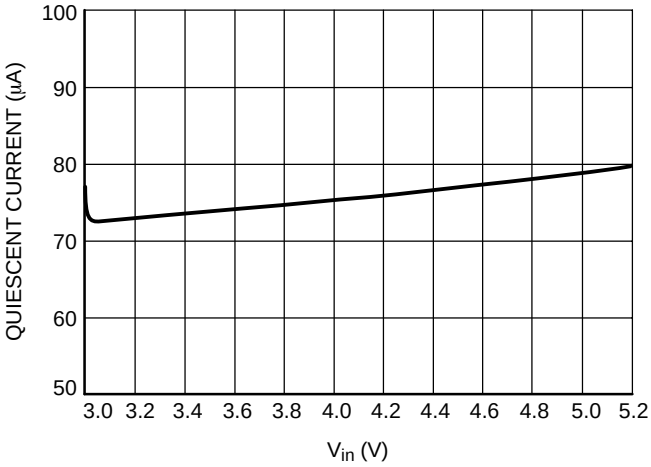


Figure 19. LDO Quiescent Current vs. Input Voltage

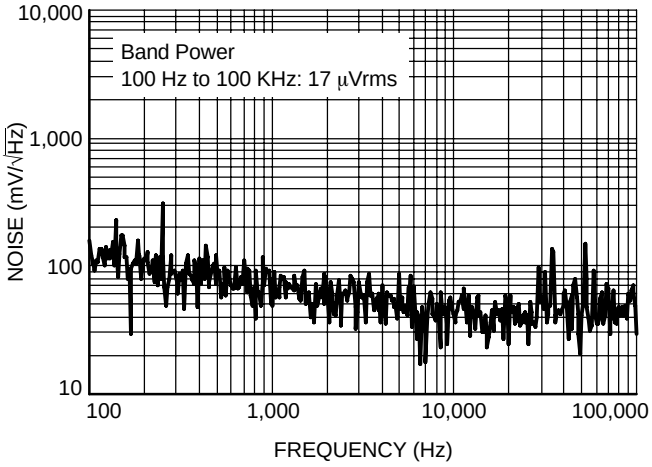


Figure 20. LDO Noise (DC/DC Converter Off)

TYPICAL CHARACTERISTICS

NCP1526 circuit on Figure 2, V_{in} = 3.6 V, T_A = 25°C, unless otherwise noted

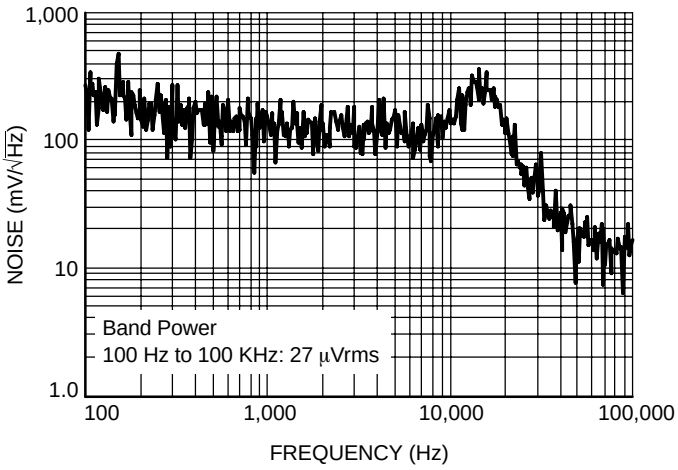


Figure 21. LDO Noise (DC/DC Converter On)

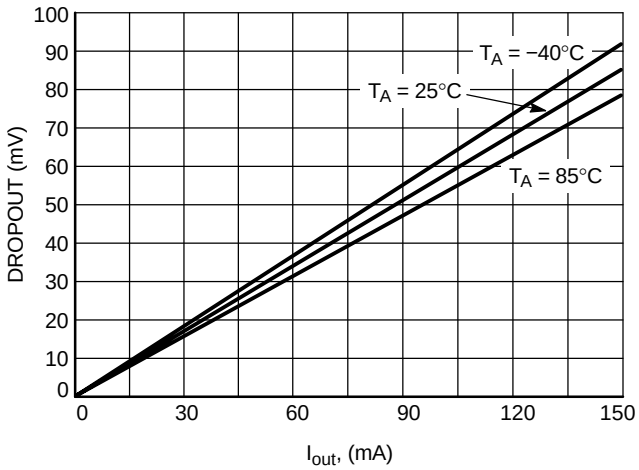


Figure 22. LDO Dropout Voltage vs. Output Current

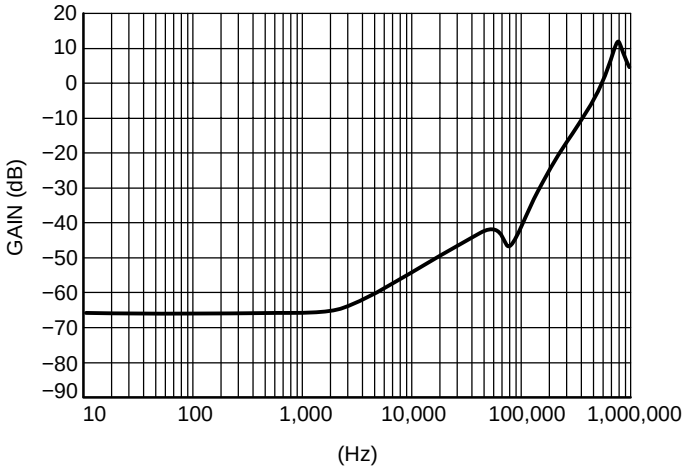


Figure 23. LDO PSRR at I_{out} = 100 μA, V_{in} = 3.6 V

DC−DC OPERATION DESCRIPTION

Detailed Description

The NCP1526 uses a constant frequency, voltage mode step−down architecture. Both the main (P−Channel MOSFET) and synchronous (N−Channel MOSFET) switches are internal.

It delivers a constant voltage from either a single Li−Ion or three cell NiMH/NiCd battery to portable devices such as cell phones and PDA. The output voltage accuracy is well within 3% of the 1.20 V. The NCP1526 can source at least 400 mA.

PWM Operating Mode

The output voltage of NCP1526 is regulated by modulating the on−time pulse width of the main switch Q1 at a fixed 3.0 MHz frequency. The switching of the PMOS Q1 is controlled by a flip−flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the PWM ramp. At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillator clock. When the PWM ramp becomes higher than the error voltage amplifier the PWM comparator resets the flip−flop, Q1 is turned OFF and the synchronous switch Q2 is turned ON. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

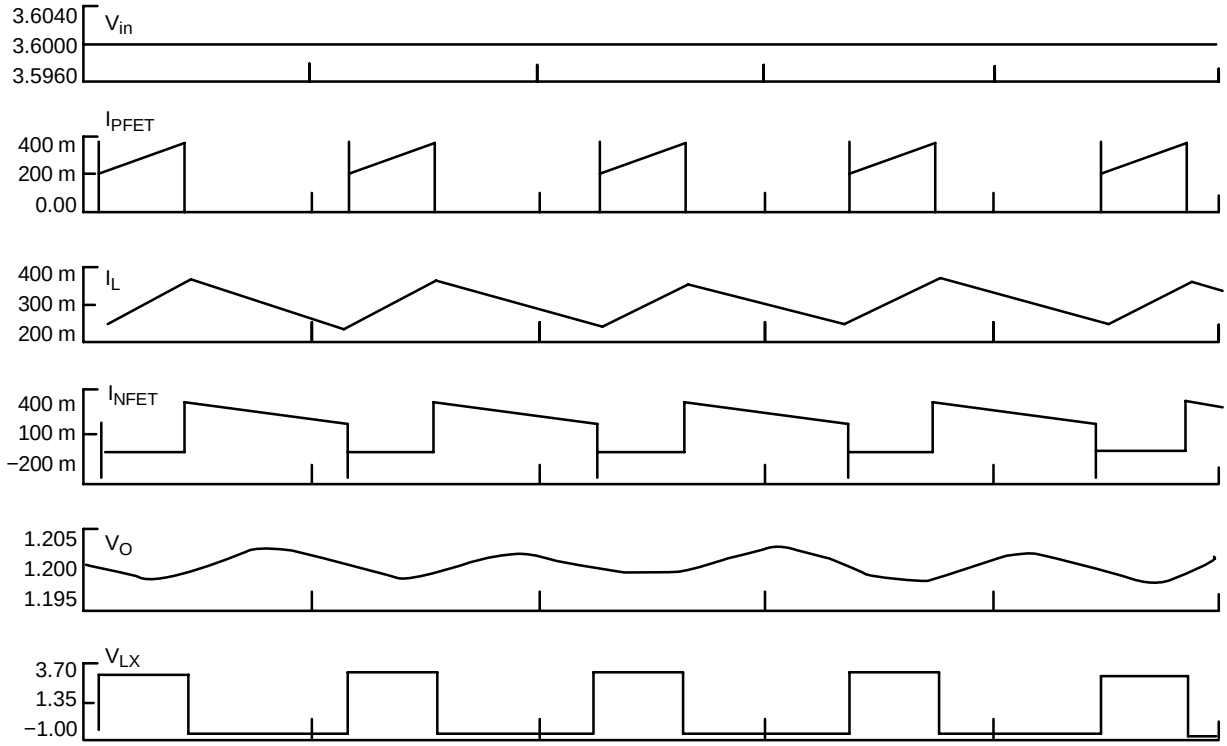


Figure 24. Waveforms During PWM Operation

Soft−Start

The NCP1526 uses soft−start to limit the inrush current when the device is initially powered up or enabled. Soft−start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft−start capacitor to provide gradually increasing reference voltage. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

Cycle−by−Cycle Current Limitation

From the block diagram (Figure 2), an ILIM comparator is used to realize cycle−by−cycle current limit protection. The comparator compares the LX pin voltage with the reference voltage, which is biased by a constant current. If the inductor current reaches the limit, the ILIM comparator detects the LX voltage falling below the reference voltage and releases the signal to turn off the switch Q1. The cycle−by−cycle current limit is set at 1000 mA (nom).

Shutdown Mode

When the EN1 pin has a voltage applied of less than 0.4 V, the DC−DC converter block will be disabled. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.2 μA (typical value). Applying a voltage above 1.2 V to EN1 pin will enable the DC−DC converter for normal operation. The device will go through soft−start to normal operation.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. If the junction temperature exceeds 160°C, the device shuts down. In this mode switch Q1 and Q2 and the control circuits are all turned off. The device restarts in soft−start after the temperature drops below 135°C. This feature is provided to prevent catastrophic failures from accidental device overheating and it is not intended as a substitute for proper heatsinking.

Undervoltage Lockout

The input voltage VIN1 must reach 2.5 V (typ) before the NCP1526 enables the DC−DC converter output to begin the startup sequence (see soft−start section). The UVLO threshold hysteresis is typically 100 mV.

APPLICATION INFORMATIONS

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is IO, max/2.

For NCP1526, a low profile ceramic capacitor of 4.7 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the VIN Pin.

Table 1. List of Input Capacitors

Murata	GRM188R60J475KE
	GRM21BR71C475KA
Taiyo Yuden	JMK212BY475MG
TDK	C2012X5ROJ475KB
	C1632X5ROJ475KT

Output L−C filter Design Considerations:

The NCP1526 is built in 3 MHz frequency and uses voltage mode architecture. The correct selection of the output filter ensures good stability and fast transient response.

Due to the nature of the buck converter, the output L−C filter must be selected to work with internal compensation. For NCP1526, the internal compensation is internally fixed and it is optimized for an output filter of L = 2.2 μH and C_{OUT} = 4.7 μF

The corner frequency is given by:

$$f_c = \frac{1}{2\pi\sqrt{L \times C_{out}}} = \frac{1}{2\pi\sqrt{2.2\ \mu H \times 4.7\ \mu F}} = 49.5\ KHz$$

The device operates with inductance value between 1 μH and maximum of 4.7 μH.

If the corner frequency is moved, it is recommended to check the loop stability depending of the output ripple voltage accepted and output current required. For lower frequency, the stability will be increase; a larger output capacitor value could be chosen without critical effect on the system. On the other hand, a smaller capacitor value increases the corner frequency and it should be critical for the system stability. Take care to check the loop stability. The phase margin is usually higher than 45°.

Table 2. L−C Filter Example

Inductance (L)	Output Capacitor (C_{out})
1 μH	10 μF
2.2 μH	4.7 μF
4.7 μH	2.2 μF

Inductor selection

The inductor parameters directly related to device performances are saturation current and DC resistance and inductance value. The inductor ripple current (ΔI_L) decreases with higher inductance:

$$\Delta I_L = \frac{V_{out}}{L \times f_{sw}}\left(1 - \frac{V_{out}}{V_{in}}\right)$$

ΔI_L peak to peak inductor ripple current

L inductor value

f_{sw} Switching frequency

The Saturation current of the inductor should be rated higher than the maximum load current plus half the ripple current:

$$I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2}$$

IL(MAX) Maximum inductor current

IO(MAX) Maximum Output current

The inductor's resistance will factor into the overall efficiency of the converter. For best performances, the DC resistance should be less than 0.3 Ω for good efficiency.

Table 3. List of Inductors

FDK	MIPW3226 series
TDK	VLF3010AT series
	TFC252005 series
Taiyo Yuden	LQ CBL2012
Coil craft	DO1605−T series
	LPO3008

Output capacitor selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode is given by:

$$\Delta V_{out} = \Delta I_L \times \left(\frac{1}{4 \times f_{sw} \times C_{out}} + ESR \right)$$

Table 4. List of Output Capacitors

Murata	GRM188R60J475KE	4.7 μF
	GRM21BR71C475KA	
	GRM188R60OJ106ME	10 μF
Taiyo Yuden	JMK212BY475MG	4.7 μF
	JMK212BJ106MG	10 μF
TDK	C2012X5ROJ475KB	4.7 μF
	C1632X5ROJ475KT	
	C2012X5ROJ106K	10 μF

OUTPUT VOLTAGE OPTIONS AVAILABLE UPON REQUEST

	DC/DC Converter
Fixed Output Voltage (V)	0.9
	1.0
	1.1
	1.2
	1.3
	1.4
	1.5
	1.6
	1.7
	1.8
	1.9
	2.5
	2.7
	3.0
	3.3

LDO Operation

Voltage Regulator V1

V1 is a 2.80 V, 3% low drop voltage regulator dedicated to RF sensitive module. It can deliver up to 150 mA and is totally protected against short to ground (current limitation) and overtemperature (thermal shutdown circuit with hysteresis).

The PSRR of the reference is in excess of 67 dB at 1.0 kHz. The output of the V1 requires a 1.0 μF capacitor for stability. An additional 100 nF capacitor is necessary on the BYPASS pin for a low output noise. If the BYPASS pin is supporting an additional load, the stability and performance of the V1 will be diminished. Since the input voltage can go as low as 3.0 V, the reference output will be affected and can drop as low as 150 mV below the input voltage at 150 mA output current. During this low dropout, the PSRR of the reference is reduced. V1 is active when logic high is applied to the EN2 pin. It is turned off by a logic low on the EN2 pin.

Reference Bypass Capacitor Node (Bypass)

An optional 100 nF BYPASS capacitor creates a low pass filter for LDO noise reduction. The output voltage noise is 45 μV_{RMS} with C_{BYPASS} = 0.1 μF and C_{OUT} = 1.0 μF. If the BYPASS pin is supporting an additional load, the stability and performance of the NCP1526 will be diminished.

Current Limiting

The output voltage regulator limits the output current to I_{SC} = 300 mA (typ). If the LDO output current exceeds I_{SC}, the output voltage drops.

Shutdown Mode

When the EN2 pin has a voltage applied of less than 0.4 V, the output voltage regulator will be disabled. In shutdown mode, the internal reference and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.2 μA (typical value). Applying a voltage above 1.2 V to EN2 pin will enable the LDO for normal operation.

OUTPUT VOLTAGE OPTIONS AVAILABLE UPON REQUEST

	LDO
Fixed Output Voltage (V)	2.5
	2.6
	2.7
	2.8
	2.85
	3.0
	3.1
	3.3

APPLICATION BOARD

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedback that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

1. Use star−ground connection to connect the IC ground nodes and capacitor GND nodes together at one point. Keep them as close as possible, and then connect this to the ground plane through several vias. This will reduce noise in the ground plane by preventing the switching currents from flowing through the ground plane.
2. Place the power components (i.e., input capacitor, inductor and output capacitor) as close together as possible for best performance. All connecting traces must be short, direct, and wide to reduce voltage errors caused by resistive losses through the traces.
3. Separate the feedback path of the output voltage from the power path. Keep this path close to the NCP1526 circuit. And also route it away from noisy components. This will prevent noise from coupling into the voltage feedback trace.

The following shows the NCP1526 demo board schematic and layout and bill of materials:

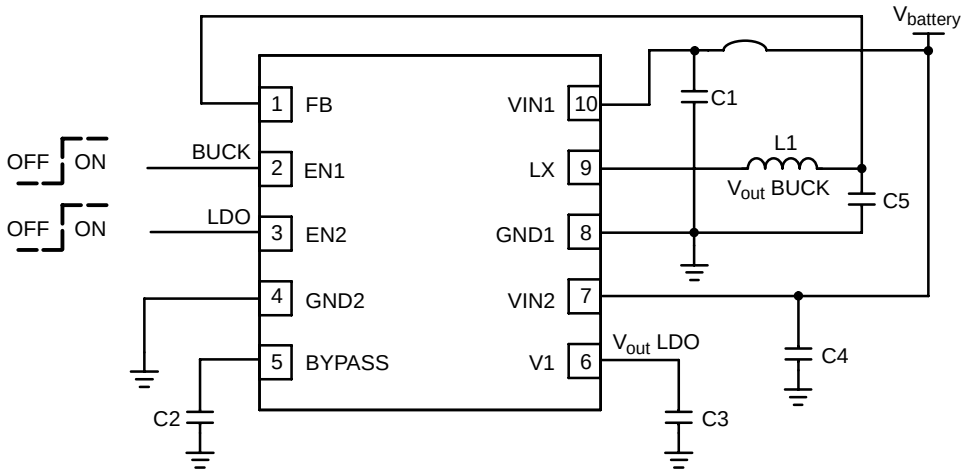


Figure 25. NCP1526 Board Schematic

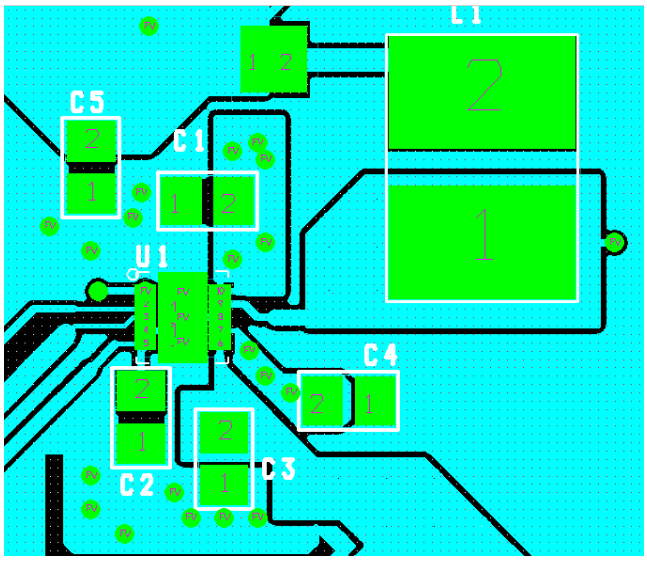


Figure 26. NCP1526 Board Layout

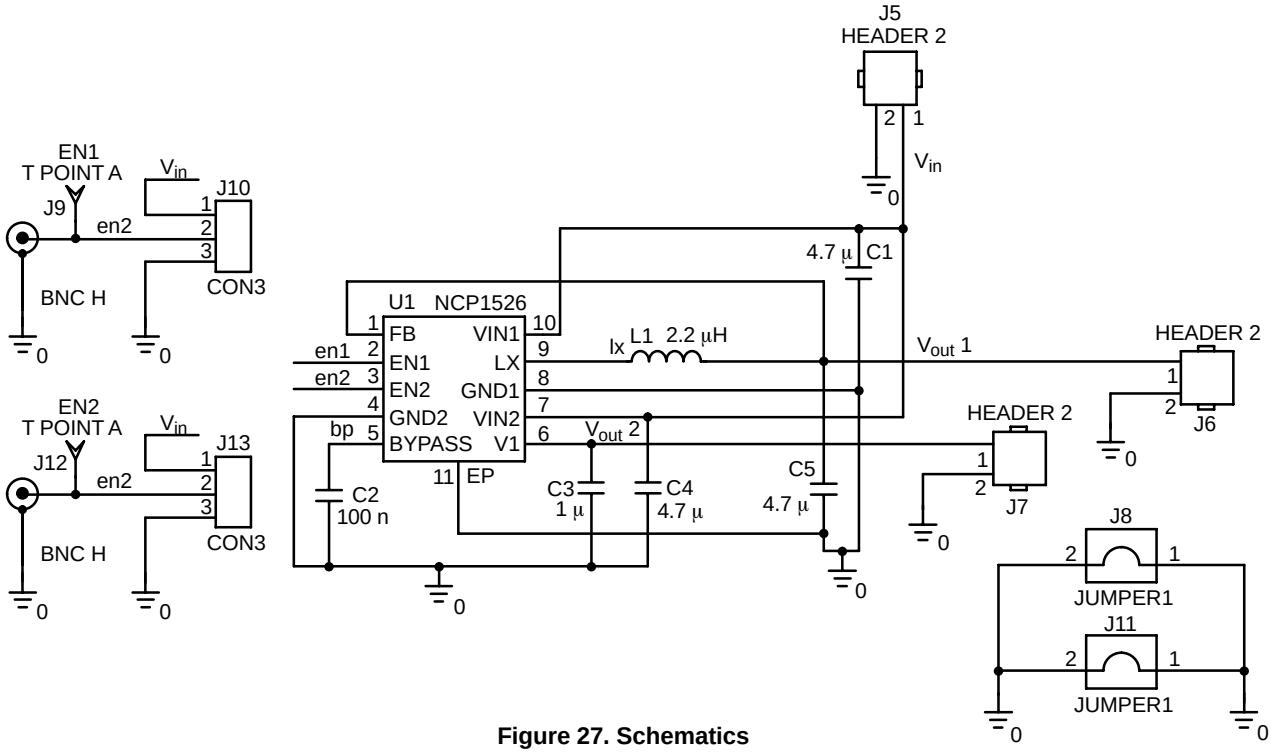


Figure 27. Schematics

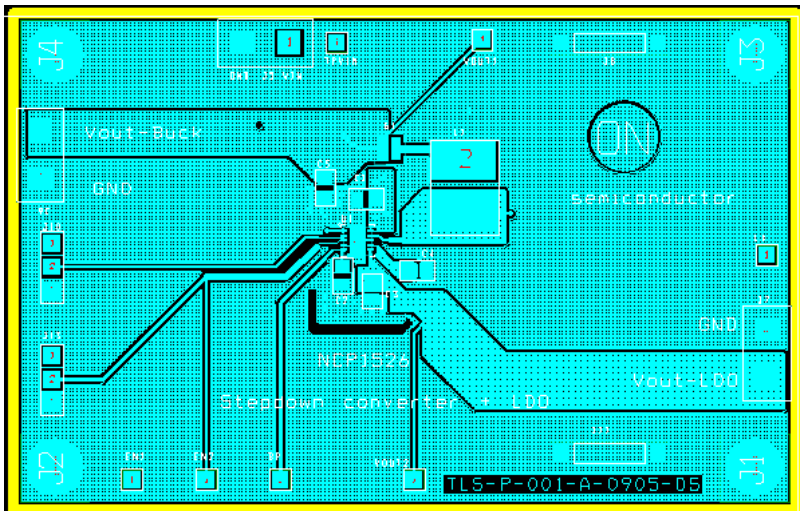


Figure 28. Board Layout (Top View)

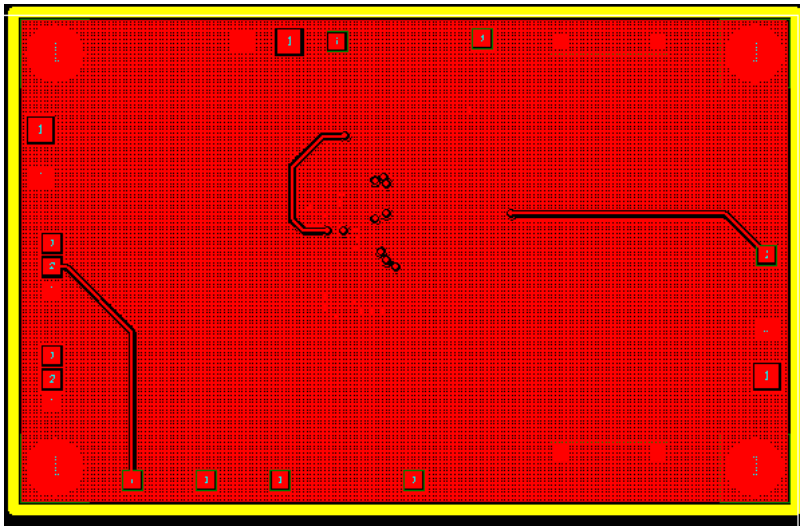


Figure 29. Board Layout (Bottom View)

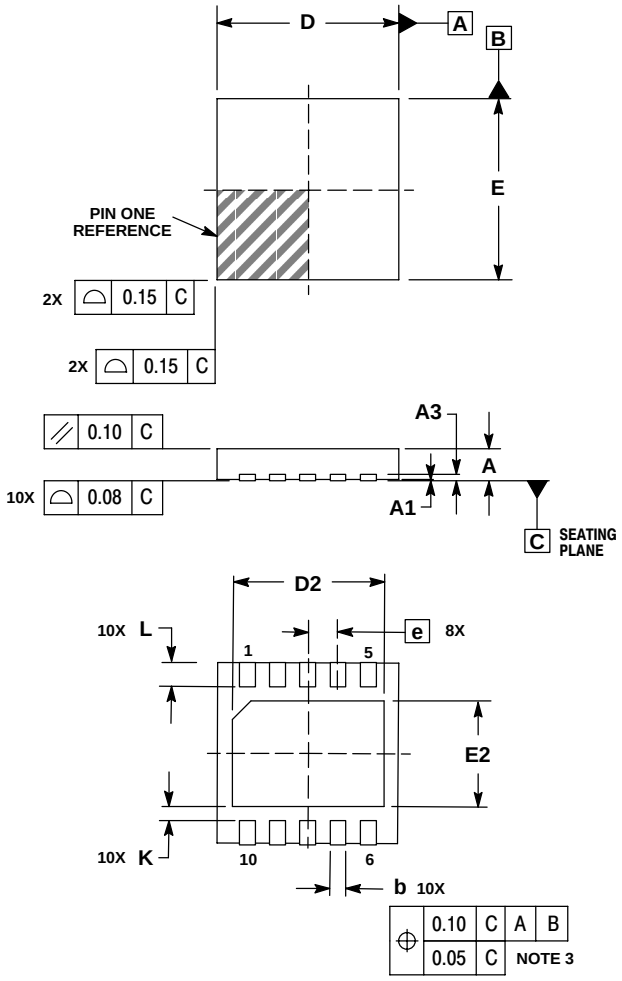
BILL OF MATERIALS

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
U1	1	IC, Converter, DC/DC	NA	NA	10−Pin DFN	ON Semiconductor	NCP1526
C1, C4, C5	3	Ceramic Capacitor	4.7 μF, 10 V, X5R	10%	0805	Murata	GRM219R61A475KE19
C3	1	Ceramic Capacitor	1 μF, 6.3 V, X5R	20%	0805	Murata	GNM212R61A105MA13
C2	1	Ceramic Capacitor	100 nF, 10 V, X7R	10%	0805	Murata	GRM219R71C104KA01
L1	1	Inductor	2.2 μH	20%	1605	Coilcraft	DO1605T−222MLB
J5, J6, J7	2	Male SL5.08/2/90B + Female BLZ5.08/2/90B Connector I/O	NA	NA	NA	Weidmuller	1510360000 + 1555060000
J10, J13	1	3 Pin Jumper Header	NA	NA	2.54 mm	TYCO/AMP	5−826629−0
J11, J8	2	Jumper for GND	NA	NA	10.16 mm	Harwin	D3082−01
EN1, EN2, VOUT_LDO, LX, TPVIN, VOUT_BUCK	6	Test Point	NA	NA	NA	Std	Std
J9, J12	0*	SMB Connector	NA	NA	NA	Radiall	R114665000
	1	88.9x61.1x1.6mm 4 Layers	NA	NA	NA	Any	TLS−P−002−A−0606−DA

*G1 is not connected on the evaluation board.

PACKAGE DIMENSIONS

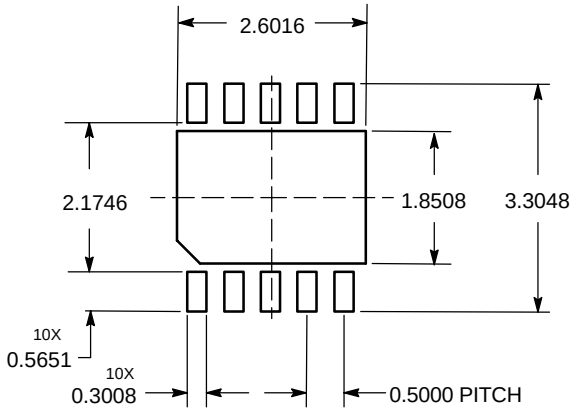
10 PIN UDFN
CASE 506AT−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.03	0.05
A3		0.127 REF	
b	0.18	0.25	0.30
D		3.00 BSC	
D2	2.40	2.50	2.60
E		3.00 BSC	
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.19 TYP	
L	0.30	0.40	0.50

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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